REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 1-22 were first objected to as allegedly being formatted in a manner not in compliance with 37 C.F.R. 1.75 and M.P.E.P. 608.01(m). In response , applicants amend each of the claims to re-format them in accordance with proper practice. The Examiner is respectfully requested to remove the objections.

Further in the Official Action, the Examiner had rejected Claims 1, 2, 7, 8, 13 and 17-19 under 35 U.S.C. §102(e) as allegedly anticipated by Nadeau-Dostie et al. (US Patent Pub. No. 2005/0047229) ("Nadeau-Dostie").

Further, Claims 3-6, 9-12, 14-16 and 20-22 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Nadeau-Dostie in further view of US Patent No. 6,978,402 to Hirabayashi ("Hirabayashi ").

As a preliminary matter, applicants hereby amend Claims 4 and 10 to remove minor typographic errors, e.g., the instance of two periods, and similarly for Claim 18 to correct spelling.

With respect to the rejection of Claims 1, 2, 7, 8, 13 and 17-19 under 35 U.S.C. §102(e) as allegedly anticipated by Nadeau-Dostie, applicants respectfully traverse in view of the amendments made herein to Claims 1, 7, 13 and 17 that distinguish the present invention over Nadeau-Dostie.

Particularly, each of Claims 1, 7, 13 and 17 are being amended to set forth an important feature of the invention, namely, that the BIST testing, performed at a multiple of an external ATE (tester) clock speed, generates a fail map data for capture by a diagnostic register device

and while the BIST testing is paused upon recognition of a fail of the embedded memory system, the external clock of the tester to read bit fail data out directly from the diagnostic register device to the tester; and then resuming the BIST testing with the high speed multiplied clock from the point at which it was paused. (Note: Claim 17, in its original form has already set forth this feature of capturing the fail map data in the same register that is used to also transfer the data to the tester.)

The additional matter added to Claims 1, 7 and 13 do not constitute new matter as the newly added diagnostic register device is the Fail Map Register 11 (see paragraph [0037] and Figs. 1, 2 and 5 of the present specification) includes all of the diagnostic latches for generation of the fail maps. What is novel in the present invention, as now claimed in amended Claims 1, 5, 7, 11, 13, 15 and 17, is that the same register (Fail Map Register 11) used to capture the failed data is the same register that is used to also transfer the data to the tester, e.g., in a serial fashion.

This is not the case in Nadeau-Dostie where the fail summary data must be transferred in a synchronous manner from a Failure Data Selector (element 178, Fig. 8 of Nadeau-Dostie) to a separate Transfer Register (element 180, Fig. 8 of Nadeau-Dostie). This separate transfer register (element 180, Fig. 8 of Nadeau-Dostie) is a separate entity clocked synchronously with a slower transfer clock. The ability to synchronously transfer the data between a fast clock and a slow clock is limited by the rate of the slow clock speed. In other words, the fail summary data must exist for a number of fast clocks equal to the period of the slow clock (if the data doesn't exist that long then data transfer is not guaranteed). This prevents fails from being captured on every fast clock cycle--after a fail is captured, no new fails can be captured until the transition is completed to the transfer register.

Thus, the key difference is that, in the present invention, the tester (e.g., external ATE) is notified of the fail, pauses test, allows the entire test circuit to transition to running off of the slow clock, and then serially unloads the data using the slow clock. The entire test circuit can then transition back to the fast clock and testing would resume when that transition is complete (following a notification from the tester).

Thus, the present invention, provides the following advantages, neither taught nor suggested by Nadeau-Dostie:

1. Full fail data (not a summary) is captured and no silicon area is wasted on a "transfer register" since the same register used to capture the fail data is also used to transfer it off chip.

2. No messy transfer of data from one clock domain to another, requiring fail data to exist for a certain number of fast clocks to ensure the transfer was successful. That is, according to the invention, new fail data can be captured on every clock cycle.

New Claims 23, 24 and 25 dependent upon Claims 1, 7 and 13, respectively, are being added to set forth this feature that new fail data can be captured on every high-speed multiplied clock cycle. Respectfully, no new matter is being added. At least one instance in the specification describes the ability of the ATE tester to shift out and collect the Fail Map data from the register 11 without disturbing the state of the BIST or the memory (see paragraph [0042] of the present specification; and at paragraph [0044] of the present specification where it is described how the system resumes BIST test from the exact point at which execution was suspended.

Moreover, note that Fig. 8 depicts signal waveforms describing the operation of the fail map circuit where two consecutive fails have been detected. Paragraphs [0060] and [0061] describe that, after BIST testing control logic switches from the tester clock back to the

multiplied clock, the macro test resumes, <u>for one cycle</u>, exactly where it left off. In this illustration, two fail net signals are consecutively generated (on an immediate multiplied clock (Clock Net) cycle) as the CFD signal is asserted (e.g., has remained high) because of the second consecutive fail.

Thus, the present invention allows for detailed fail data to be captured on any cycle (including back to back cycles) due to the data being captured in the same register that is used to also transfer the data to the tester.

The applicant submits that amended Claims 1, 5, 7, 11, 13, 15 and 17 set forth novel subject matter as each element is neither taught nor described by Nadeau-Dostie whether taken alone or in combination with Hirabayashi.

With respect to the rejection of Claims 3-6, 9-12, 14-16 and 20-22 under 35 U.S.C. §103(a) as allegedly unpatentable over Nadeau-Dostie in further view of Hirabayashi Applicants respectfully submit that Hirabayashi does not make up the deficiencies of Nadeau-Dostie. Hirabayashi simply describes how to generate multiplied clocks and select between them. The key to the present invention is implementing a circuit/method that allows a tester to interact with the test circuitry across an asynchronous interface to recognize fail data is available, stop test, switch clocks (as Hirabayashi may describe) and synchronously unload the data without requiring a complicated data synchronizing state machine, or an extra transfer register, as required by the teachings of Nadeau-Dostie.

Thus, in view of the foregoing, the Examiner is respectfully requested to withdraw the rejections of Claims 1, 2, 7, 8, 13 and 17-19 under 35 U.S.C. §102(e) and, additionally, withdraw the rejections of Claims 3-6, 9-12, 14-16 and 20-22 under 35 U.S.C. §103(a).

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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